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IEEE STD IEEE Standard

 1. Frequent loop detection using efficient nonintrusive on-chip hardware

Gordon-Ross, A.; Vahid, F.;  
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Henkel, J.; Ernst, R.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 9, Issue 2, April 2001 Page(s):273 - 289  
Digital Object Identifier 10.1109/92.924041[AbstractPlus](#) | [References](#) | [Full Text: PDF\(464 KB\)](#) [IEEE JNL](#)**IEEE CNF** IEE Conference Proceeding**IEEE STD** IEEE Standard**2. A configurable logic architecture for dynamic hardware/software partitioning**

Lysecky, R.; Vahid, F.;

Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings Volume 1, 16-20 Feb. 2004 Page(s):480 - 485 Vol. 1  
Digital Object Identifier 10.1109/DATE.2004.1268892[AbstractPlus](#) | [Full Text: PDF\(243 KB\)](#) [IEEE CNF](#)**3. Hardware/software partitioning of embedded systems with multiple hardware processes**

Hendry, D.C.; Sananikone, D.S.;

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[AbstractPlus](#) | [Full Text: PDF\(984 KB\)](#) [IEE JNL](#)**4. An approach to hardware/software partitioning for multiple hardware devices model**

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Digital Object Identifier 10.1109/SEFM.2004.1347542[AbstractPlus](#) | [Full Text: PDF\(923 KB\)](#) [IEEE CNF](#)**5. Area/delay estimation for digital signal processor cores**

Miyaoka, Y.; Kataoka, Y.; Togawa, N.; Yanagisawa, M.; Ohtsuki, T.;

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Togawa, N.; Sakurai, T.; Yanagisawa, M.; Ohtsuki, T.;  
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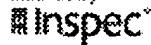
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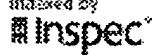
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IEEE STD IEEE Standard

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Edwards, M.; Fozard, B.;  
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 Integrated Circuits and Systems Design, 2002. Proceedings. 15th Symposium on  
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... configuration data of an **FPGA**-like device that is used to **accelerate** the decoding.  
... **Profiling** of the **code** on the target processor provides either the ...  
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You can implement custom hardware **acceleration** with a discrete **FPGA** interfaced to a  
... After identifying what **code** to **accelerate** and deciding whether to ...  
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Although the insertion of **profiling code** can slow and intrusively affect the  
application performance, it will, as a first approximation, locate the main **hot** ...  
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First, the software developer identifies **hot spots** using Stretch's **profiling tool**.

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LabVIEW **FPGA** Module includes an Interrupt function, shown in Figure 7, to facilitate

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... tool generates the framework for source **code** and the **profiling** tool uncovers

... CoDeveloper provides C to RTL design and compilation for various **FPGA** ...

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are not accurate due to the insertion of **profiling code** into the application.

System level. simulation provides a more accurate way of determining **hot spots** ...

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